PSG INSTITUTE OF TECHNOLOGY AND APPLIED RESEARCH

In association with
SANDISK
organizes

HACKATHON

 # An intensive hackathon for multi-track engineering talent

Prize Pool

₹ 150K

Idea evaluation by Industry experts and Academicians

DESIGN DEEP, THINK SMART.

Where logic flows and machine minds grow.

 # Hard Logic

 # Smart Results

HACKATHON SCHEDULE

- **March 16 , 2026**
  Idea Submission Deadline (Round 1 - Online)
- **March 20, 2026**
  Announcement of Round 1 results (Online)
- **March 27 & 28 , 2026**
  The Grand Finale of Hackathon in PSG iTech(Offline)

Registration is limited to the **first 100 teams.**
Entries will be accepted on a **first-come, first-served** basis.

SCAN TO REGISTER

& access the detailed problem statement.

TEAM SIZE : **Maximum 4 per team**
(Interdisciplinary teams are encouraged)

WHO CAN APPLY : **Students currently pursuing B.E. / B.Tech**

This hackathon challenges students to integrate hardware design with machine intelligence, covering semiconductor lifecycle, computer vision, RISC-V architecture, firmware optimization, and AI-driven chip verification.

TRACKS AVAILABLE

TRACK 1 : AI/ML

Theme 1 : Image-Based Wafer Map Pattern Intelligence

Objective : Apply AI/ML techniques to classify and interpret wafer map patterns. Use computer vision and deep learning to analyze wafer images (e.g., component defects, board-level issues) and predict potential failures before they occur, improving defect localization and yield optimization.

Theme 2 : AI-Enabled Functional Coverage Prioritization

Objective : Use AI to identify coverage gaps and prioritize specific coverage bins or random seeds to close verification faster under tight schedules.

Theme 3 : AI-Enabled Debug Prioritization

Objective : Build an analysis tool for simulation logs that identifies unique failures and categorizes them (UVM, SVA, etc.) to accelerate debug closure.

TRACK 2 : FIRMWARE

Theme : Firmware Algorithms, Efficiency and Reliability (SSD / NAND)

Objective : Enhance SSD firmware performance and field reliability by implementing optimized data structures for bad-block metadata management and logic minimization techniques like K-map and Quine-McCluskey for embedded systems.

TRACK 4 : RTL – Verification

Theme 1 : Failure Prediction from Historical Data

Objective : Develop an AI-based tool to forecast future bug trends using project history, aiding in resource planning and tapeout readiness decisions.

Theme 2 : Automatic Delta-Change Verification Planning

Objective : Create an AI-assisted tool to analyze design changes, identify impacted verification sections, and automatically propose required plan updates.

Theme 3 : Bug Bounty – End-to-End Challenge

Objective : Verify a provided design and specification to identify the maximum number of functional and corner-case bugs while highlighting specification mismatches.

TRACK 3 : RTL – Design

Theme 1 : Heuristic RTL Analysis Tool

Objective : Build an intelligent analysis tool/script to suggest power-reduction optimizations and identify unsafe clock domain crossings (CDC) or coding style issues.

Theme 2 : Packet Parser & Router

Objective : Create a hardware module capable of extracting header fields, validating checksums, and routing packets based on destination or priority fields.

Theme 3 : Protocol Transaction Monitor

Objective : Build a synthesizable checker to verify protocol rules (like VALID/READY handshakes) during simulation or FPGA prototyping while tracking latency and throughput.

Theme 4 : Intelligent Memory Architect (IMA)

Objective : Develop a software-based (Python/TCL) generator that parses user parameters to output fully synthesizable and power-optimized memory controller RTL.

Theme 5 : 3-Stage Pipelined Instruction Decoder

Objective : Design a hardware decoder to process an 8-bit serialized stream and execute READ/WRITE/ERASE commands through a static memory interface.

Theme 6 : RISC-V plus In-Memory Compute (IMC)

Objective : Define the pipeline behavior and triggering mechanisms for a 5-stage RISC-V CPU connected to an SRAM-based IMC unit for analog MAC operations.

Theme 7 : Co-Design of Custom ISA and ReRAM IMC

Objective : Integrate a ReRAM crossbar compute model with ISA-level control so specialized compute operations can be invoked and retired correctly within the RTL.

For Queries Contact :

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